

## IN THE CLAIMS

1. (Currently amended) A track and hold circuit (1) comprising: a linear amplifier (2) receiving a differential analog signal ( $D+$ ,  $D-$ ) and being controlled by a first binary clock signal ( $H+$ ) having a first phase and a second phase, the linear amplifier (2) providing a feed-forward input signal substantially equal with the differential analog signal ( $D+$ ,  $D-$ ), a pseudo latch circuit (3) being controlled by a second binary clock signal ( $H-$ ) for memorizing the feed forward input signal and for providing a differential output signal ( $LD+$ ,  $LD-$ ) substantially equal with the feed-forward input signal during the second phase of the first binary clock signal ( $H+$ ), the second binary clock signal being substantially in anti-phase with the first binary clock signal ( $H+$ ).
2. (Currently amended) A track and hold circuit (1) as claimed in claim 1, wherein the linear amplifier (2) comprises a first common source pair of transistors ( $T1$ ,  $T2$ ) biased in their common source terminals by a ~~switchable~~switchable current source ( $I_{sub,DC}$ ) via a first switch ( $S1$ ) controlled by the first binary clock signal ( $H+$ ) and receiving at their gates the differential analog signal ( $D+$ ,  $D-$ ), the linear amplifier (2) further comprising a common drain transistor ( $T3$ ) having a gate coupled via substantially equal resistors ( $R$ ) to the gates of the first common source pair of transistors ( $T1$ ,  $T2$ ) for determining drain currents flowing through the pair of transistors ( $T1$ ,  $T2$ ).
3. (Currently amended) A track and hold circuit (1) as claimed in claim 1, wherein the pseudo latch circuit (3) comprises a second common source pair of transistors ( $T4$ ,  $T5$ ) being biased in their common source terminals by a ~~switchable~~switchable current source

~~(I<sub>sub</sub> DC)~~ via a second switch (~~S2~~) controlled by the second binary clock signal (~~H~~) and receiving at their gates the signal provided by the linear amplifier (~~2~~), the pseudo latch circuit (~~3~~) further comprising a common drain transistor (~~T6~~) having a gate coupled via substantially equal resistors (~~R<sub>g</sub>~~) to the respective gates of the second differential transistor pair (~~T4, T5~~) for reducing bias currents through the second transistor pair (~~T4, T5~~), the second transistor pair (~~T4, T5~~) being cross coupled.

4. (Currently amended) A track and hold circuit (~~1~~) as claimed in claim 2, wherein the linear amplifier (~~2~~) further comprises a pair of capacitors cross-coupled between a drain of a transistor of the first transistor pair (~~T1, T2~~) and the gates of the other transistor of the first transistor pair (~~T2, T1~~), respectively for reducing crosstalk currents at the amplifier's output.

5. (Currently amended) A track and hold circuit (~~1~~) comprising a cascaded coupling of two substantially identical linear amplifiers (~~2~~) as claimed in claim 4, for better isolating the input data from the pseudo latch circuit (~~3~~).

6. (Currently amended) A tracking data cell (~~10~~) comprising a pair of track and hold circuits (~~1, 1'~~) as claimed in claim 1 coupled to a first multiplexer (~~5~~), a clock signal (~~H+~~, ~~H~~) being inputted substantially in anti-phase in the respective track and hold circuits (~~1, 1'~~) for determining a receipt of a data signal (~~D+~~, ~~D~~) having a rate, said track and hold circuits (~~1, 1'~~) providing an output signal (~~Q~~) having a substantially half rate.

7. (Currently amended) A Phase Locked Loop comprising a first tracking data cell ~~(10)~~ and a second tracking data cell ~~(10')~~ as claimed in claim 6 receiving an input signal ~~(D+, D-)~~ and being controlled by a respective quadrature clock signals ~~(Hi, Hq)~~ generated by a voltage controlled oscillator ~~(VCO)~~, the first tracking data cell ~~(10)~~ being coupled to a hard ~~limiter~~ limiter ~~(11)~~ providing a binary data out signal ~~(DO)~~, the second tracking data cell being coupled to a delay element ~~(12)~~ providing an input signal for a pair of track and hold circuits ~~(1, 1')~~, the track and hold circuits being controlled by the binary output signal ~~(DO)~~ and providing a frequency correction signal ~~(E)~~ for the voltage controlled oscillator ~~(VCO)~~ via a low-pass filter ~~(LPF)~~.

8. (Currently amended) A Phase Locked Loop comprising a first tracking data cell ~~(10)~~ and a second tracking data cell ~~(10')~~ as claimed in claim 6 receiving an input signal ~~(D+, D-)~~ and being controlled by a respective quadrature clock signals ~~(Hi, Hq)~~ generated by a voltage controlled oscillator ~~(VCO)~~, the first tracking data cell ~~(10)~~ being coupled to a hard ~~limiter~~ limiter ~~(11)~~ providing a binary data out signal ~~(DO)~~, the second tracking data cell being coupled to a delay element ~~(12)~~ providing an input signal for a pair of track and hold circuits ~~(1, 1')~~, the track and hold circuits being controlled by the binary output signal ~~(DO)~~ and providing a frequency correction signal ~~(E)~~ for the voltage controlled oscillator ~~(VCO)~~ via a low-pass filter ~~(LPF)~~ further comprising a frequency error detector comprising an input circuit ~~(50)~~ including: a first track and hold circuit ~~(30)~~ and a second track and hold circuit ~~(30')~~ as claimed in claim 1, receiving the frequency correction signal ~~(E)~~ and being controlled by the binary output signal ~~(DO)~~, said first and second track and hold circuits ~~(30, 30')~~ being coupled to a multiplexer means ~~(25)~~ controlled by

the binary output signal ~~(DO)~~, the multiplexer means ~~(25)~~ being coupled to a slicer ~~(35)~~ providing a signal which is subtracted from the frequency correction signal ~~(E)~~ in a subtractor ~~(S)~~, the subtractor ~~(S)~~ providing a signal ~~(FD)~~ indicative for a frequency error between the frequency correction signal ~~(E)~~ and the binary output signal ~~(DO)~~.

9. (Currently amended) A phase detector comprising a first input circuit ~~(500)~~ and second input circuit ~~(500)~~ as claimed in claim 8, first and second input circuits ~~(500, 500)~~ receiving respective quadrature clock signals ~~(Hq, Hh)~~, being controlled by input data signal ~~(D)~~ and providing respective first output signal ~~(A)~~ and second output signal ~~(B)~~, the first output signal ~~(A)~~ and its inverse replica being inputted to an output multiplexer ~~(OM)~~ controlled by the second output signal ~~(B)~~ via a hard ~~limiter~~ limiter ~~(250)~~ and providing a signal ~~(PD)~~ indicative for a phase error between the input data signal and clock signal.